Two-Stage MPPT Power Regulator for Satellite Electrical Propulsion System

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A novel DC-DC power converter has been developed to fulfill the requirements of a solar electrical propulsion module. The maximum power point tracker solar array regulator is divided into two series converters; a direct-energy transfer (DET) regulator and a secondary step-up converter. The DET regulator creates an unregulated maximum power point bus and the secondary converter regulates to a 100-V bus. The purpose of this paper is to describe the solution with a specific design and experimental results.

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I. INTRODUCTION

Nowadays, the development of electrical spacecraft propulsion (EP) systems has been stimulated by the limitations in conventional chemical propulsion. Chemical propulsion systems are limited by the available reaction energies, and thermal transfer considerations limit exhaust gas velocities to a few thousand meters per second. However, many desirable future space missions require an alternative source of energy and higher velocities. For these missions EP offers these possibilities [1]. Although EP has been used for station keeping and orbit adjustments since the early eighties, its use as a primary means of propulsion has been restricted until now. Recently, the European Space Agency (ESA) has promoted the use of EP for geostationary satellites and interplanetary missions, e.g., Alphabus (Large Platform Telecommunication Mission) [2], Smart-I [3], or BepiColombo [4].

BepiColombo is an ambitious scientific ESA mission in cooperation with Japan that will explore Mercury, the planet closest to the Sun. The main power source will be a 14-kW solar array that must be conditioned to obtain a 100-V regulated bus to feed the EP engine and some ancillary equipment. The interplanetary journey will force very extreme conditions for the solar power generation, changing the electrical characteristics of the solar array (SA). Therefore the use of a maximum power point tracker (MPPT) has been addressed because it is essential for this mission. Moreover, the harsh conditions that the SA will be exposed to also suggest a modular electrical architecture to assure minimum power losses in case of failure.

Additionally the particular requirements of the EP load must be taken into consideration, and these are more stringent than a typical spacecraft. The EP is subject to so-called beam out effect, which represents a transient switching from on to off, or vice versa, of the EP engine in a matter of a few microseconds [5]. The effect of an ion-engine switch off is tantamount to going from full to almost zero load, and the power system must be designed to minimize the resulting transient voltage on the bus. The European Space Agency power standard [6] imposes a maximum overvoltage of 1% of the nominal bus voltage when a sudden load change of 50% occurs. This fixes an overvoltage of less than 2% during the "beam out" and imposes a low-impedance bus.

To summarize, the main features of the BepiColombo solar array regulator are

—Modular and MPPT electrical architecture.
—High voltage (100 V)/low impedance regulated bus.
—Input voltage (SA voltage) in the range 57–93 V.
—Estimated SA power around 14 kW.

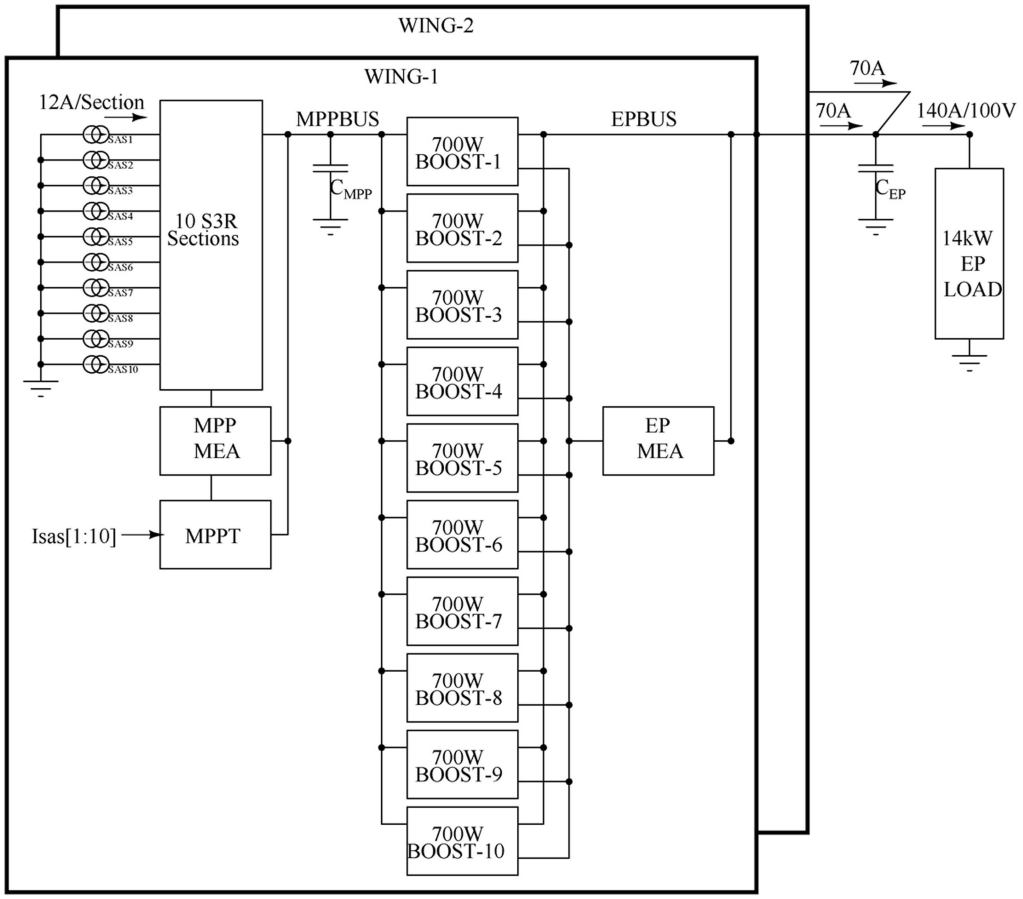

Fig. 1. The BepiColombo proposed PCDU.

—Optimization of the electrical subsystem mass and cost.

—If possible, optimization of the electrical subsystem heritage.

A two-stage solar array regulator has been proposed for this application to the European Space Agency (ESA) under contract with Alenia Spazio in the framework of the BepiColombo mission. This power converter has been presented in [7–9], and it is based, as shown in Fig. 1, on a two-stage DC/DC converter: a sequential switching shunt maximum power regulator (S3MPR) [10, 11] plus a step-up (Weinberg) regulator [12, 13]. The S3MPR is a sequential switching shunt regulator (S3R) with the ability to keep the SA voltage at its MPP (53–93 V), creating an intermediate and low-impedance bus (named MPP bus). The Boost regulators are fed from the MPP bus to produce the regulated 100-V output voltage required for the EP bus. For the MPPT control technique, a variation of the classical perturb and observe (P&O) algorithm has been selected. This variation improves efficiency under constant irradiance conditions and is well suited for the interplanetary journey.

Although the S3R and the Weinberg regulator have been widely used in aerospace power systems [14, 15], the S3R always has been used as a solar array regulator without MPPT capabilities, and the Weinberg converters are usually used as battery discharge regulators. The use of an S3R as an MPPT regulator is quite different in concept from any previous MPPT designs [16, 17]. Therefore, the purpose of this paper is to describe the detailed design and the experimental results of a scaled-down prototype (1 kW of output power) of the new system. This prototype is made up of four solar array sections conditioned by four S3R cells, feeding an MPP bus and two Weinberg Boost converters (see Fig. 2).

The results prove than this new concept satisfies the requirements of the BepiColombo high power EP in an innovative and reliable solution.

II. SEQUENTIAL SWITCHING SHUNT MAXIMUM POWER REGULATOR (S3MPR) CONVERTER DESIGN

The basic specifications of the S3MPR prototype are presented in Table I; some of them are fixed by the ESA standards and can be found in [6].

Component sizing and control loop design follows the guidelines given in [10, 18]. The only difference with the classical regulator design is that the voltage reference is no longer constant but is made proportional to the voltage at which MPP

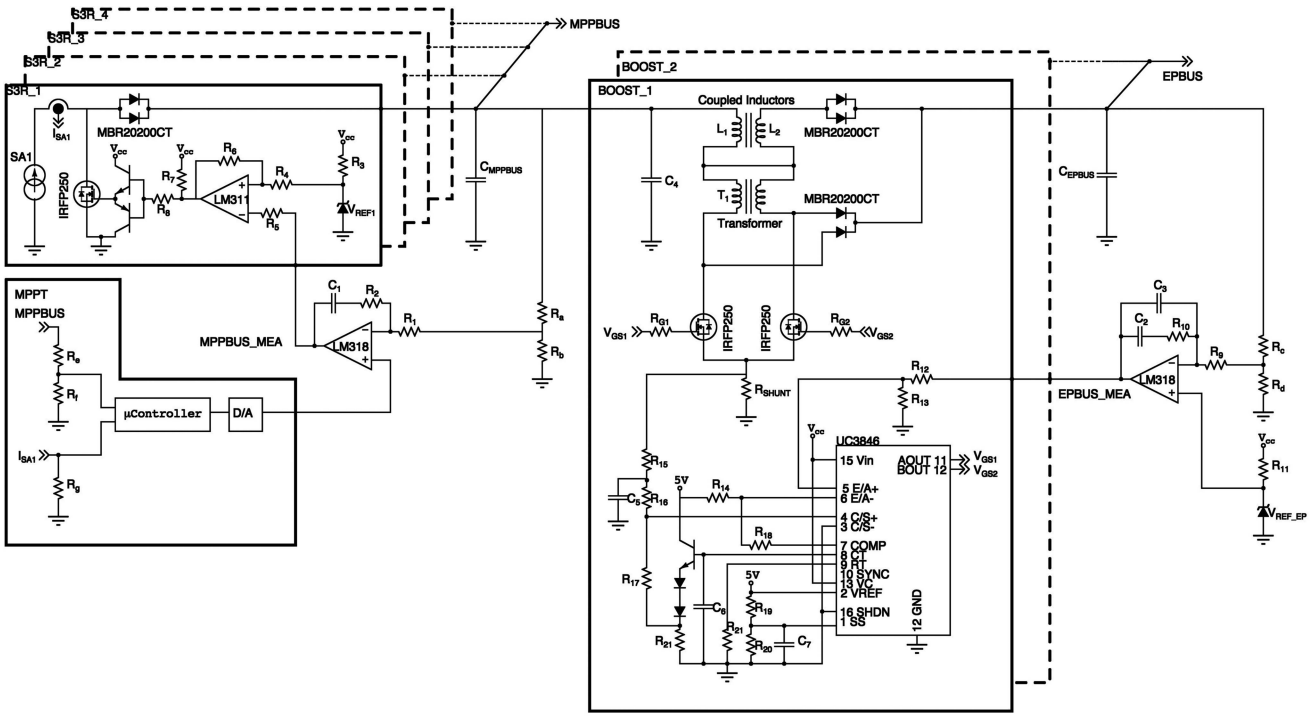

Fig. 2. 1-kW BepiColombo PCDU prototype.

TABLE I
S3MPR and MPP Bus Specifications

Solar Array (Agilent Solar Array Simulators E4351B used)	
Solar array voltage (V_{MPP})	57–93 V
SAS short circuit current (I_{SC})	4 A
SAS MPP current (I_{MPP})	3.75 A
Output impedance	< 250 mΩ
Phase margin	$> 60°$
Minimum gain margin	10 dB
MPP bus voltage ripple	< 1 V
Power stage conductance (G_{SAR})	3.75 A/V
S3R maximum switching frequency	< 2.5 kHz

occurs. To achieve a breadboard that is close to a real converter, we have taken special care to use electronic components with associated space-qualified counterparts, but at the proof of concept level neither redundancy nor protection circuits have been considered. Fig. 2 shows the schematic of the designed S3MPR.

The MPP bus capacitance has been selected as 480 μF and the design considers low ESL and ESR, applying a special layout and low-capacitance high-performance capacitors (48 capacitors/10 μF MKP EPCOS, model B32669, 250 V). The power devices selected for the S3MPR cells are IRFP250 MOSFET and dual Schottky rectifier MBR20200CT.

Because the S3MPR uses a hysteretic controller for each power cell, a simple linearization of the cascaded power cells is used for the control loop design (see Fig. 3).

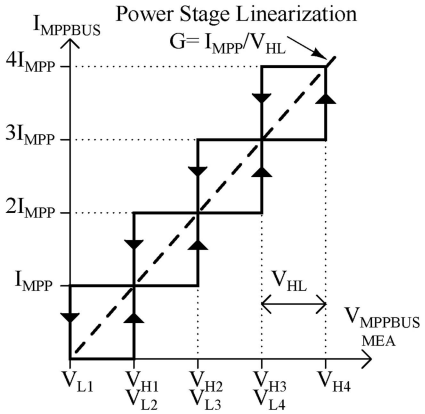

Fig. 3. S3MPR power cells linearization.

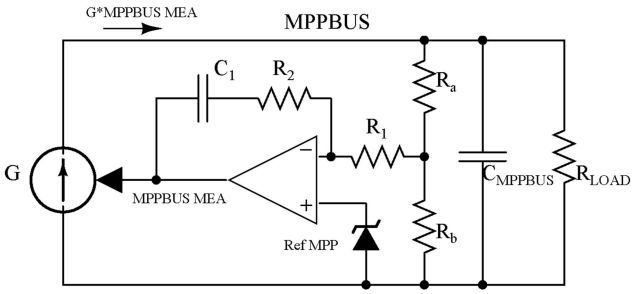

Fig. 4. S3MPR linear model.

As a result, the model of the converter corresponds to a current-voltage controlled source that feeds a first order output filter (see Fig. 4). The detailed calculations of the MPPBUS control loop design can be found in the Appendix.

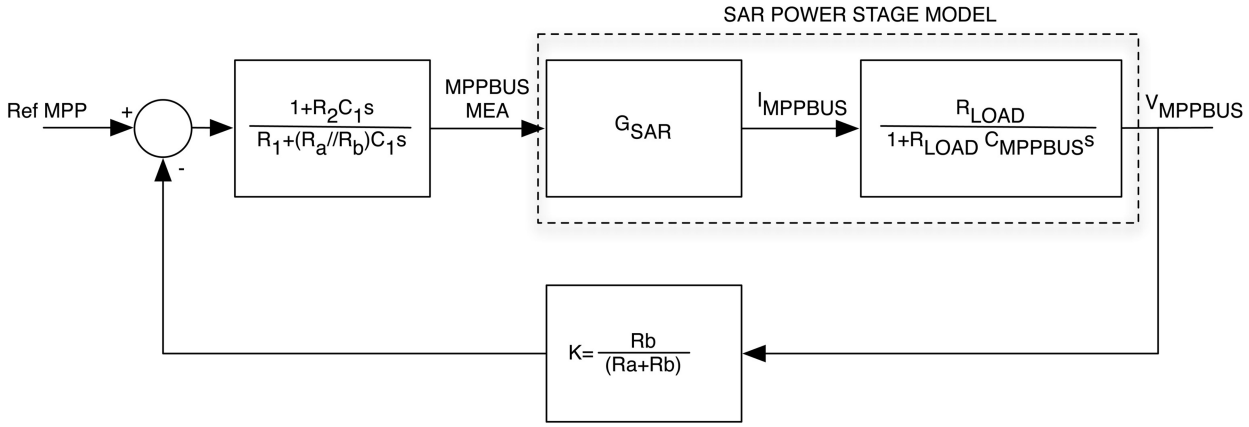

Fig. 5. System block diagram used to deduce transfer function $T(s)$.

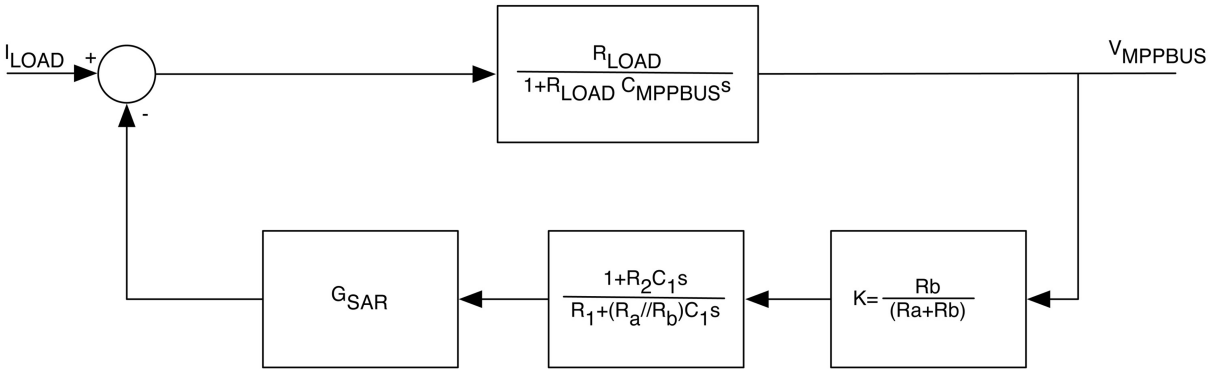

Fig. 6. System block diagram used to deduce closed-loop output impedance.

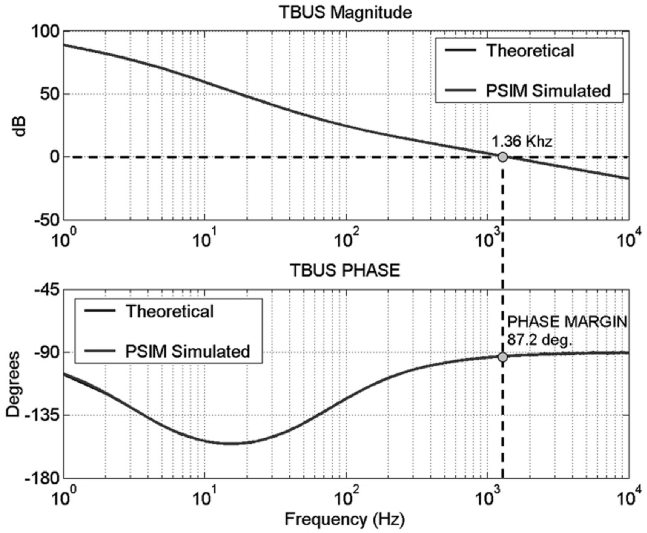

Fig. 7. Theoretical and simulated loop gain transfer function $T(s)$.

Block diagrams shown in Figs. 5 and 6 are used to derive the system loop gain, $T_{\mathrm{MPPBUS}}(s)$ and the closed loop output impedance, $Z_{\mathrm{OMPPBUS}}(s)$, of the S3MPR converter.

From the analysis of these diagrams, (1) and (2) are deduced, and their graphical representation is shown in Figs. 7 and 8.

$$T_{\mathrm{MPPBUS}}(s) = K \cdot G_{\mathrm{SAR}} \frac{1 + R_2C_1s}{R_1 + (R_a//R_b))C_1s} \cdot \frac{R_{\mathrm{LOAD}}}{1 + R_{\mathrm{LOAD}}C_{\mathrm{MPPBUS}}s} \tag{1}$$

$$Z_O(s) = \frac{1}{K \cdot G_{\mathrm{SAR}}} \cdot \frac{R_1 + (R_a//R_b))C_1s}{(1 + R_2C_1s) \cdot \left(1 + \dfrac{((R_1 + (R_a//R_b)) \cdot C_{\mathrm{MPPBUS}})}{K \cdot G_{\mathrm{SAR}} \cdot R_2}s\right)}. \tag{2}$$

Although the hysteretic modeling of the power stage differs from the PWM control, Figs. 9 and 10 show PSIM [19] simulated and experimental results with very good agreement with respect to the theoretical model. In particular, Fig. 9 shows the response of the linear and the switched models. The voltage overshoot that takes places in the intermediate MPPBUS is approximately 2.2 V in a 10-A step load change.

III. MPPT CONTROL DESIGN

For the MPPT circuit, a modification of the well-known digital perturb and observe [20, 21] has been selected. The variation included is based on the addition of a waiting function that stops the perturbations if the sign of the perturbation is

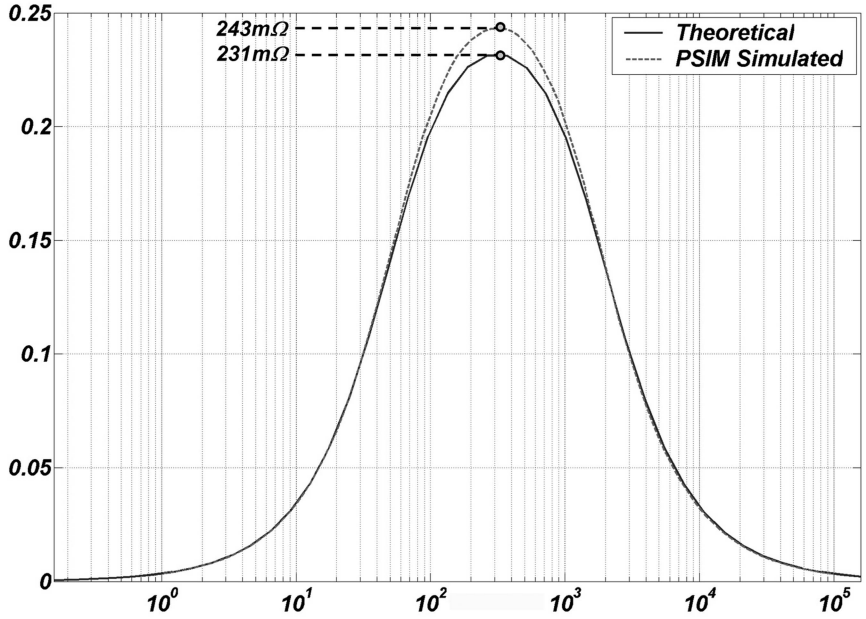

Fig. 8. Theoretical and simulated S3R output impedance.

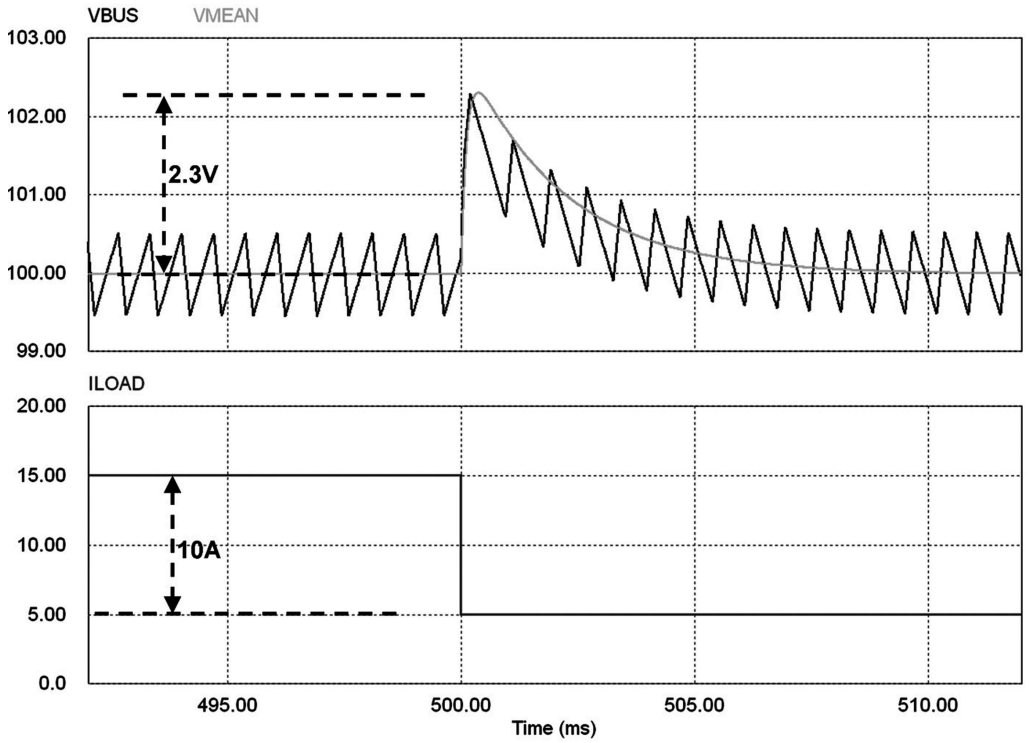

Fig. 9. Simulation of S3MPPR 10A load change. Upper trace: MPPBUS voltage (linear and switched model); lower trace: load current.

reversed several times [22]. Using this modification, we see that the MPP bus voltage remains constant until a change in the SA power is detected or a preprogrammed timeout is raised, avoiding oscillations around the MPP. This feature increases the MPPT efficiency during the interplanetary journey to Mercury because the solar arrays will remain under illumination most of the time, and it is expected that the MPP voltage will change very slowly.

For testing purposes, the digital perturb and observe with waiting function (DP&OW) algorithm has been programmed in an 8-bit microcontroller. It is worth noting that a real digital MPPT detector should be designed with qualified FPGA circuitry; however, for the sake of simplicity, a low cost, easy-programmable microcontroller has been used and again redundancy is not considered. A Hall effect current sensor (LEM LA55-P/SP1) was used for breadboarding purposes. Sensed points are converted

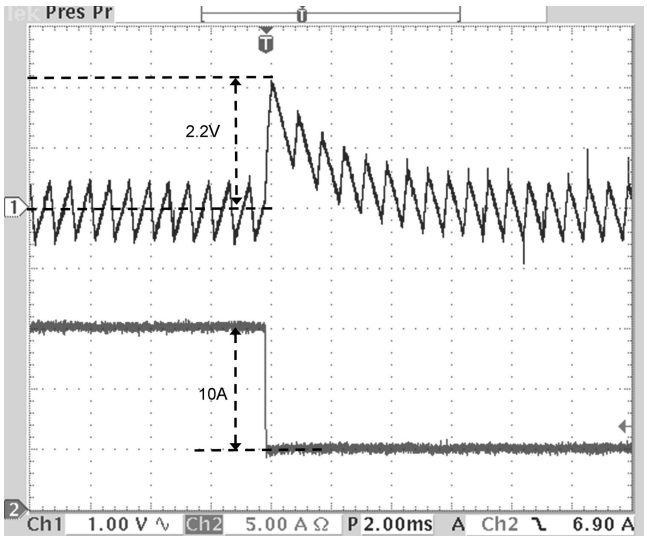

Fig. 10. Experimental results of S3MPPR 10 A load change. Upper trace: MPPBUS voltage; lower trace: load current.

into digital signals through two A/D 10-bit converters that are internal to the microcontroller. The resultant MPPT output signal is converted into an analog signal with a 12-bit D/A converter.

The algorithm compares the power just sensed with the result obtained in the previous measurement. Depending on the result, the MPPT output, which is the reference of the voltage regulation loop, increases or decreases its value until the system oscillates around the MPP. Once the algorithm detects several oscillations around the MPP, it stops perturbations until a power change or after a preprogrammed timeout is raised.

The S3MPR and the MPPT algorithm behaviors have been fully simulated using PSIM software. The digital MPP model has been programmed in C and has been linked to the simulator using a dynamic link library. The preprogrammed MPP BUS voltage step determines the accuracy and the dynamic response of the MPPT. As long as the P-V curve of a solar panel can be supposed to be a symmetrical parabola near the MPP point and taking into account the output ripple of the S3MPR, the maximum voltage error of the MPPT algorithm is given by (3):

$$V_{\mathrm{MPPERROR}} = \frac{V_{\mathrm{STEP}}}{2} + \frac{\Delta V_{\mathrm{MPPBUS}}}{2}. \tag{3}$$

Lower voltage steps give higher accuracy MPP tracking but result in slow dynamic response when solar array conditions change. Higher voltage steps deal in fast dynamic response but also exhibit poor MPP accuracy tracking. The MPPT accuracy has been fixed at 2% of the minimum voltage (V_{MPPBUS} = 57 V).

$$V_{\mathrm{MPPERROR}} \leq 57\ \mathrm{V} \cdot 0.02 = 1.14\ \mathrm{V}. \tag{4}$$

TABLE II
Weinberg Boosts Specifications

Peak Current Mode Control	
Input voltage (V_i)	57–93 V
Output voltage (V_o)	100 V ± 1%
Output voltage ripple	< 1 V
Output power (P_o)	0.5 kW
Output impedance (Z_{OMAX})	< 125 mΩ
Phase margin	> 60°
Minimum gain margin	10 dB
Efficiency	> 96%
Switching frequency	100 kHz

Final selection of the bus voltage step, V_{STEP}, was 1 V, resulting in a maximum MPP tracking error of 0.9875 V, i.e., less than 1.75% of the lowest MPP voltage. As observed in Fig. 9, the waiting function stops the perturbations if the sign of the perturbation is reversed six times consecutively. To avoid possible interferences with the MEA control loop [23, 24], we have designed the MPPT with a long time constant MPP refreshment (20 ms). The slow dynamic response of the MPPT loop ensures that the MPP voltage is not affected, to any degree, by sudden load changes, e.g., the full load to no load transients that are experienced during the beam-out of the EP. Fig. 11 shows the simulation results of the S3MPR controlled by the DP&OW algorithm.

IV. WEINBERG BOOSTS DESIGN

The Weinberg Boost modules convert the MPP voltage into a 100 V ± 1% regulated voltage required for the EP load. The basic specifications of each of the two parallel Weinberg Boosts designed are presented in Table II.

Schematic of each of the boost regulators is shown in detail in Fig. 2. The push/pull FET's Q1 and Q2 are PWM controlled to regulate the peak current in them. The regulator produces continuous output current. The design shown is for 100-kHz operation, which gives a 200-kHz current ripple operation. The MOSFETS and diodes selected for Boosts are the same as the ones selected for the S3MPR (IRFP250, MBR20200CT) and each Weinberg Boost converter has been controlled by a Texas Instrument PWM controller IC UC3846 using peak current control.

For the design of the input inductors $L1$ and $L2$, a ripple current that will be 30% of the maximum output current is selected. This high current ripple is allowed because the MPP bus capacitance has very low ESL and ESR to accomplish with the ESA standards, and allows minimizing the size and the efficiency of the Weinberg input inductors. In the Weinberg converter, the maximum current ripple

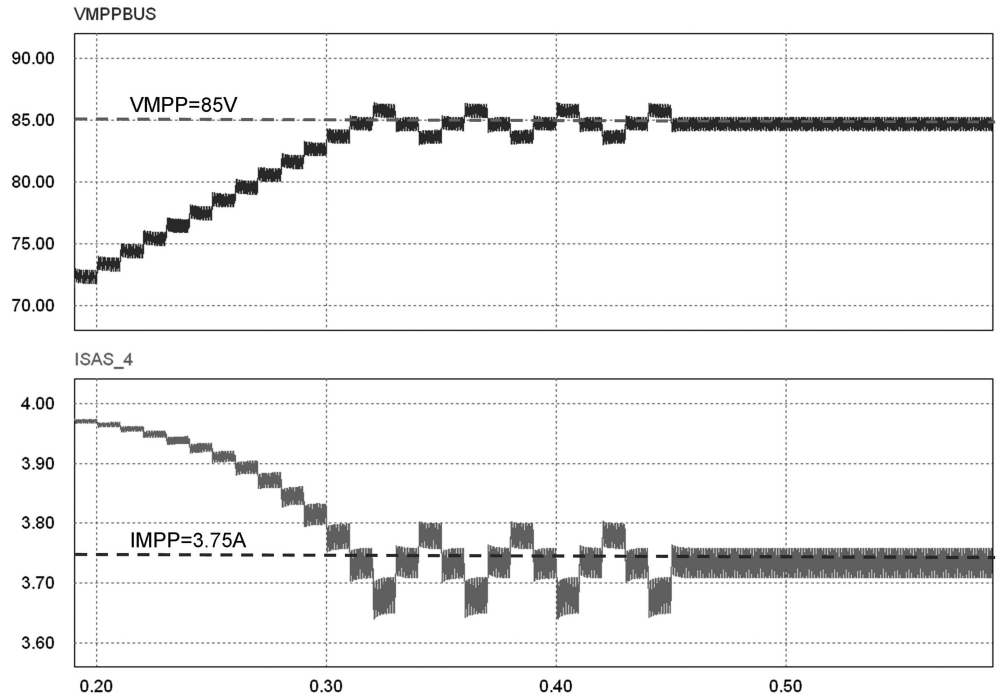

Fig. 11. S3RMPR PSIM simulation. Upper trace: MPPBUS voltage; lower trace SAS1 current.

appears when the duty cycle is 41% [11]; then the value of each inductor is

$$L = \frac{V_{\mathrm{OUT}}}{4 \cdot \Delta I_{\mathrm{OUT}} \cdot f_s} \cdot \left(\frac{2D}{1+D} - D \right) \approx 14.8\ \mu\mathrm{H}. \quad (5)$$

$L1$ and $L2$ coupled inductors have been implemented in core shape RM10 using material 3F3 with 8 turns of 12 wires of AWG26 in the primary and 8 turns of 10 wires of AWG29 in the secondary. The maximum estimated losses in the core are 0.259 W and in the copper 0.504 W.

The value of the magnetizing inductance (L_m) of the transformer T2 has to accomplish $L_m \gg L$ to minimize the magnetizing current. The transformer is designed with $N_p = N_s$ and $L_m = 450\ \mu$H. The transformer has been implemented in core shape RM10 using material 3F3 with 9 turns of 0.1×8 mm copper sheet in the primary and the secondary. The maximum estimated losses in the core are 0.302 W and in the copper 0.472 W.

For the calculation of the output capacitance (C_{ep}) the maximum output impedance (Z_{OMAX}) is considered. If a theoretical cut-off frequency of the voltage loop (f_{bw}) equal to 10 kHz is selected, the output capacitance is equal to

$$C_{\mathrm{EPBUS}} \geq \frac{1}{2 \cdot \pi \cdot f_{\mathrm{BW}} \cdot Z_{\mathrm{OMAX}}} \approx 127\ \mu\mathrm{F}. \quad (6)$$

A combination of two 65 μF/160 V AVX-FFV3 capacitors in parallel has been chosen.

Peak current control has been applied to each Weinberg converter following the design criteria applied to a typical buck configuration. Peak current mode control can be easily implemented by sensing the addition of currents across each switch with a small sensing resistor Rs. This current is the same as the output current, but spikes are not present because of the transformer leakage inductance. The need for filtering the sensed current is implemented with an RC network. This RC filter not only filters out the noise but also brings many stability problems, especially if a large duty ratio cycle range is needed. The main reason for it is the severe distortion of the sense current waveform that results in an excessive phase loss because the slope of the filtered current sensed is very different from the ideal one. This phase loss is much higher than the one expected from the filter itself. The problem becomes worse if the duty cycle is reduced and if the load is increased. As a result, cycle skipping appears for low output current and high input voltage. Because the simple peak current control is not able to guarantee stability over the entire input voltage range (huge duty cycle range), another solution was tested (different current sensing method). In this case, a Hall-effect current sensor (LEM LA55-P) with a bandwidth of 200 kHz has been used for sensing the inductor's currents. With this solution the current waveforms sensed have a triangular shape and therefore does not present any steep edge. In this way the RC noise filter does not distort the sensed waveform or degrade the phase margin when the duty cycle is very small. To avoid instabilities for $D > 50\%$, we must add a ramp to the current sensed.

To design a proper compensation to the system, we must take into account that a Weinberg Boost converter can be modeled as a Buck converter with an equivalent output inductor ($L_{eq} = 4L$). Because we have two Weinberg Boost converters in parallel, the system behaves as two equivalent Buck converters in parallel, each one with an output inductor (L_{eq}).

The two equivalent Buck converters can be modeled as an only Buck converter with an equivalent sensing resistance and output inductor that has half the value of the ones of each converter ($R_{s\_eff} = R_s/2$ and $L_{eff} = L_{eq}/2$).

An integrator network compensator of two poles and one zero has been used to implement the gain of the main voltage error amplifier (MEA) (see Fig. 2.)

The control-to-output current transfer function, which represents the power stage, is

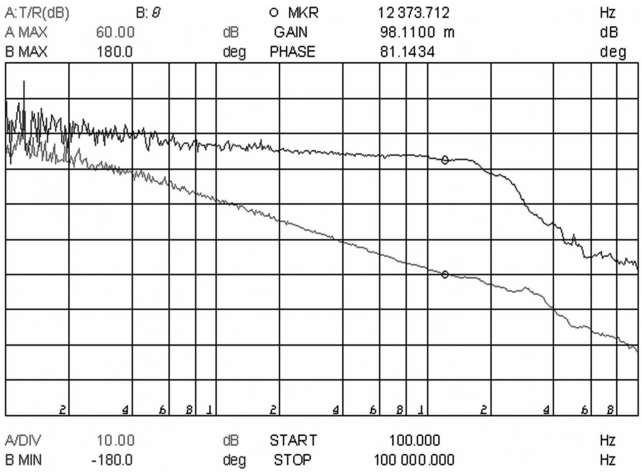

Fig. 12. Frequency response of two Boost EP regulators in parallel.

$$P(s) = \frac{V_{MPPBUS}}{R_{EPLOAD}} \left[\frac{1 + (R_{EPLOAD} + R_c) \cdot C_{EPBUS} \cdot s}{4L_1 \cdot C_{EPBUS} \cdot \left(1 + \frac{R_c}{R_{EPLOAD}}\right) \cdot s^2 + \left(R_c \cdot C_{EPBUS} + \frac{4L_1}{R_{EPLOAD}}\right) \cdot s + 1} \right] \tag{7}$$

where R_{EPLOAD} is the load resistor, C_{EPBUS} the bus capacitor, and R_c the equivalent series resistor of C_{EPBUS}.

The proportional gain of the MEA to achieve the desired bandwidth (f_{bw}) has been calculated. The pole w_p of the control transfer function is canceled with the zero of the MEA to increment the gain at low frequencies and to cancel the stationary error. To mitigate the ESR effect of the C_{EPBUS}, the second pole of the MEA is chosen at the same frequency as the zero formed by ESR and C_{EPBUS}.

Fig. 12 shows the dynamic response of the EP bus. In that case, the two Weinberg converters are working in parallel, obtaining a bandwidth of 12.3 kHz with a phase margin of 81° for 1 kW output power and 75 V input voltage.

V. EXPERIMENTAL RESULTS

Fig. 13 shows the final prototype layout; the proposed regulator has been extensively tested in the laboratory using four solar array simulators (Agilent Solar Array Simulators E4351B) as the power source.

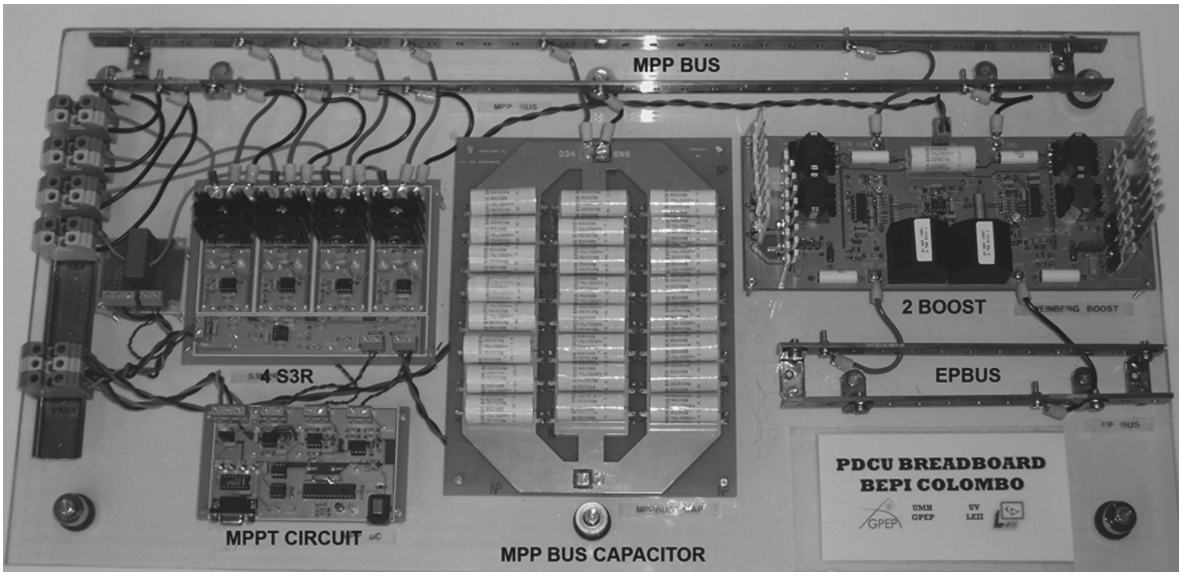

Fig. 13. Prototype test setup layout.

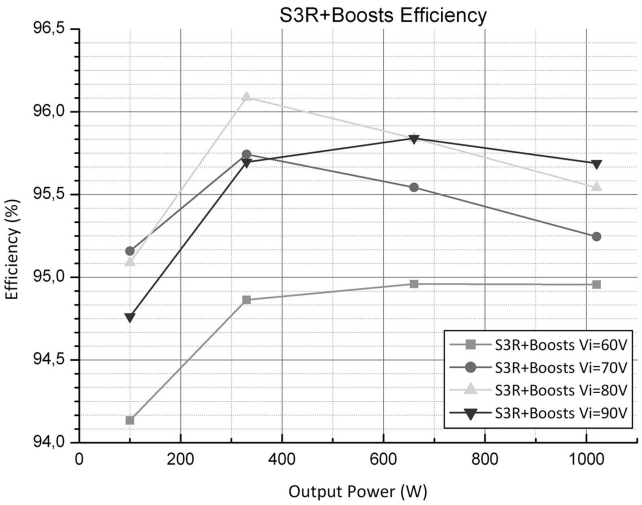

Fig. 14. Measured PCDU efficiency.

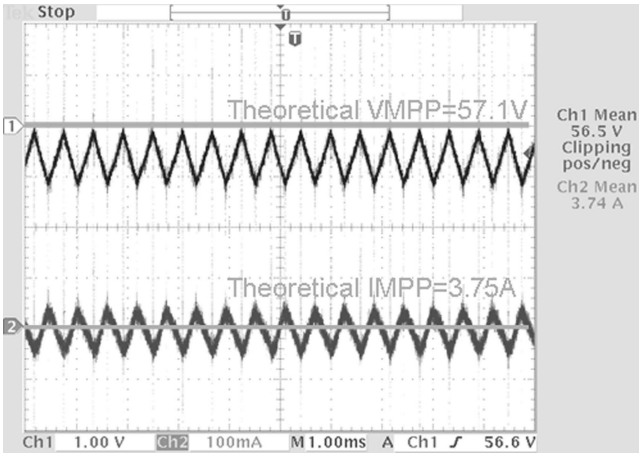

Fig. 15. MPP steady state example. MPP bus voltage (upper trace); SAS1 current (middle trace).

The measured efficiency can be seen in Fig. 14. The worst efficiency of the whole converter is 94.1% for minimum input voltage and minimum output power. The best system efficiency is 96.1%.

The MPPT was designed to expect a maximum voltage error of 0.987 V. Fig. 15 shows the MPP bus voltage in steady state conditions; this figure corresponds to the lowest MPPT efficiency measured. Under these conditions, the MPPT has stopped its oscillations and only the S3R ripple appears. The measured MPPT efficiency in this case is 98.6%.

To emulate the transient behavior of the MPPT, several *I-V* curves on the simulator have been used. Fig. 16 shows the main variables when a change between two preprogrammed curves (curve 1: V_{MPP} = 57 V, I_{MPP} = 3.75; curve 2: V_{MPP} = 75 V, I_{MPP} = 3.75) suddenly occurs. The robustness of the MPPT algorithm can be observed. It remains at the MPP of curve 1 (zone A); it starts the acquisition of the new MPP (curve 2) in zone B; it maintains the perturbation of the MPP bus voltage in zone C;

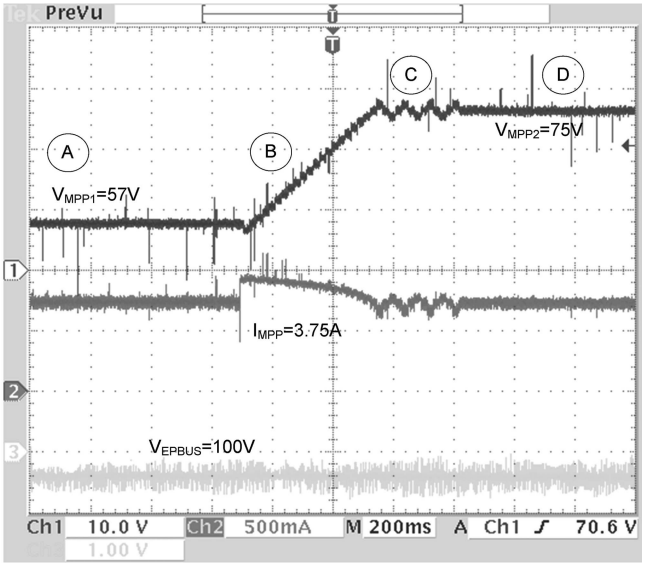

Fig. 16. MPP update example. MPP bus voltage (upper trace); SAS1 current (middle trace); EP bus voltage (lower trace).

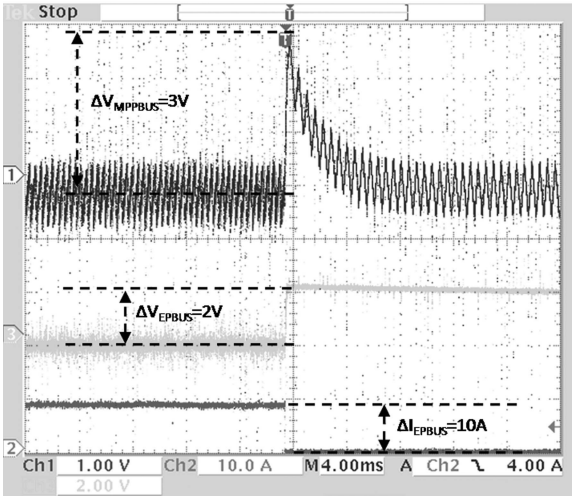

Fig. 17. EP BUS beam-out effect. MPP bus voltage (upper trace); EP bus voltage (middle trace); load current (lower trace).

and finally, it applies the waiting function in zone D, keeping the average bus voltage to the new V_{MPP}. Moreover, during all this time the main 100-V bus remains unchanged.

One of the severe working conditions is the sudden switch-off of the SEP load (beam-out effect). A full load switch-off (1 kW, from 10 to 0 A) has been applied to the prototype (see Fig. 17). The MPP bus (75 V) reacts in such a way that the solar array power is shunted, the EP output overvoltage is around 2 V, and the MPP voltage is not affected.

VI. CONCLUSIONS

A two-stage solar array regulator has been proposed, designed, and tested for high power EP loads. The presented solution has the following advantages.

- It uses well-known and established regulation units as building blocks. These units have already been used on regulated bus systems with 30 years' heritage.
- With the architecture chosen, the S3MPR independently controls the MPP voltage and the Boosts independently control the EP voltage. This makes the design very simple, predictable, and robust.
- It has a very high bandwidth. The speed of to-load changes is so fast than even for a 100% load change, the EP bus maintains the ESA regulated bus specifications.
- The operation at the MPP of the SA is an approach that is different from the traditional MPPT converters. Therefore it is not required to continuously modulate the SA power around its maximum point to find the MPP, and the SA sections that are supplying power are always operating at their MPP independently of load. Moreover, the digital MPPT detector improves tracking efficiency under steady-state illumination conditions.
- A new MPP algorithm (DP&OW) has been tested. With this algorithm, the control of the MPP voltage can be more accurate than a conventional MPP system because the update of the reference MPP voltage coming from MPPT does not have to be adjusted very often. Because the MPP bus differs slightly from regulated busses, this approach can be extended to other spacecraft power applications. In particular, it can be of interest in future telecommunication platforms.

APPENDIX

For the MPPBUS MEA design, the following guidelines have been applied:

1) Define the feedback network constant (K). K depends on the MPP reference voltage used. The maximum reference voltage that can provide the MPP circuit is 10 V. The final value of K has been selected so the MPP circuit can control the MPP bus voltage from 57 to 93 V (8).

$$K = \frac{V_{\mathrm{REFMPP}}}{V_{\mathrm{MPPBUS}}} = \frac{R_b}{R_a + R_b} = \frac{6\ \mathrm{k\Omega}}{56\ \mathrm{k\Omega} + 6\ \mathrm{k\Omega}} = 0.0968. \tag{8}$$

2) Define the hysteresis window of the hysteresis controllers. If the upper limit of the k cell is equal to the lower limit of the $k+1$ cell, the gain of the complete solar array is equivalent to the gain of a simple cell, as represented in Fig. 3.

$$V_{\mathrm{HL}} = \frac{I_{\mathrm{MPP}}}{G_{\mathrm{SAR}}} = \frac{3.75A}{4\ \mathrm{A/V}} = 0.9375\ \mathrm{V}. \tag{9}$$

3) Select the minimum gain of the PI compensator. The minimum value has to take into account the maximum impedance of the MPP bus:

$$A_{\mathrm{SAR}} > \frac{1}{K \cdot G_{\mathrm{SAR}} \cdot Z_{\mathrm{OMAX}}} = \frac{1}{0.0968 \cdot 4\ \mathrm{A/V} \cdot 250\ \mathrm{m\Omega}} = 10.34. \tag{10}$$

Choosing $R_2 = 68\ \mathrm{k\Omega}$ and $R_1 = 1\ \mathrm{k\Omega}$.

$$A_{\mathrm{SAR}} = \frac{R_2}{R_1 + (R_a // R_b)} = 10.59. \tag{11}$$

4) Calculate the bus voltage ripple and the crossover frequency.

$$\Delta V_{\mathrm{MPPBUS}} = \frac{V_{\mathrm{HL}}}{K \cdot A_{\mathrm{SAR}}} = \frac{0.9375\ \mathrm{V}}{0.0968 \cdot 10.34} = 0.937\ \mathrm{V}. \tag{12}$$

$$f_{c\mathrm{S3MPPR}} = \frac{G_{\mathrm{SAR}} \cdot K \cdot R_2}{2\pi \cdot (R_1 + (R_a // R_b)) \cdot C_{\mathrm{MPPBUS}}} = 1.36\ \mathrm{kHz}. \tag{13}$$

5) Select the value of C_1. The value is selected to assure a large phase margin ($> 60°$). The zero frequency is placed two decades below the crossover frequency.

$$C_1 = \frac{20}{2\pi \cdot f_{c\mathrm{S3MPPR}}} \approx 33\ \mathrm{nF}. \tag{14}$$

6) Calculate the maximum switching frequency.

$$f_{\mathrm{Switch}} = \frac{0.25 \cdot K \cdot A_{\mathrm{SAR}} \cdot G_{\mathrm{SAR}}}{C_{\mathrm{MPPBUS}}} = 2.135\ \mathrm{kHz} \tag{15}$$

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